



General Description:

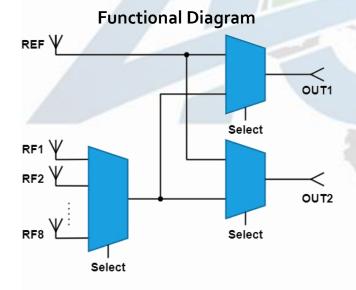
Carousel is a a switching element designed for direction finding applications. It consists of an 8 to 2 multiplexing switch network combined with a 1 to 2 switch. This setup allows users to compare a reference input to one of 8 array inputs.

The configurable single board computer controls various modes of switching behavior. Also offers the option to run custom software.

Features:

- 20MHz to 6000MHz frequency coverage
- Bypassable, 20dB amplifiers at the outputs
- Gateworks GW7100 Embedded SBC
- 1G Ethernet (including Power over Ethernet)
- Debug interface (JTAG and UART)
- GPIO interface (3.3V tolerant)
- Calibration port for internal path measurement
- Antenna array ready



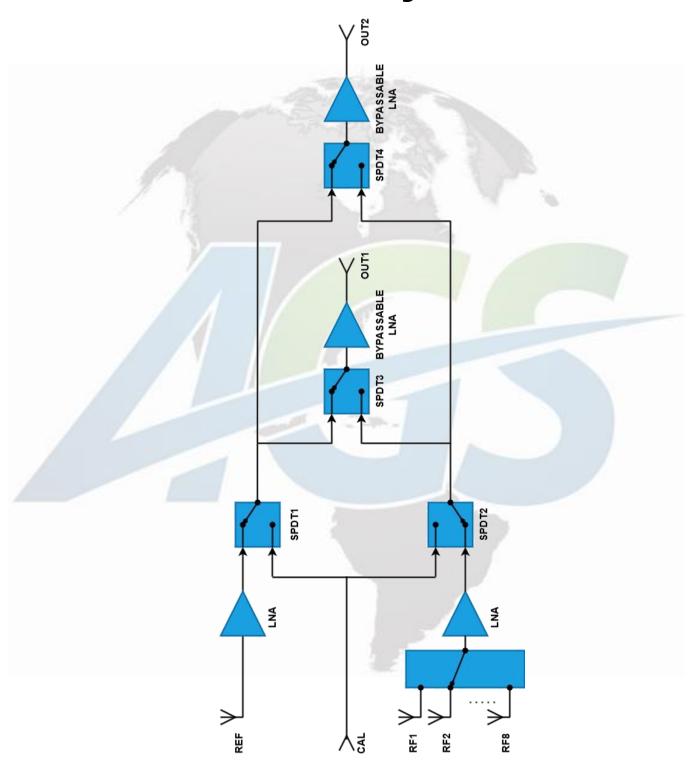


Specification Sheet (Reference Only)			
Index	Parameter	Information	
1	Frequency Range	20 MHz to 6GHz	
2	Absolute Max RF Power	0dBm	
3	Noise Figure	<tbd></tbd>	
3	RF Connectors	SMA Jack	
4	Switching Time	< 3ms	
7	Voltage Input	8 - 60V	
8	Typical Power	5W @ 24V	
9	Dimensions	4.5" x 5.25" x 2"	
10	Weight	<tbd></tbd>	

PRELIMINARY



RF Block Diagram



PRELIMINARY





Debug Connector

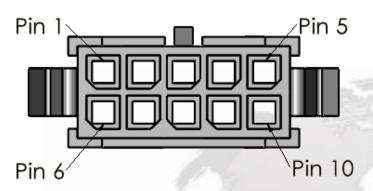


TABLE A: DEBUG PIN OUT		
PIN	SIGNAL	
1	RESET	
2	TDO	
3	UART RX	
4	TCK	
5	UART TX	
6	TMS	
7	GROUND	
8	TDI	
9	3.3 V	
10	TRST	

The debug connector provides a JTAG and UART interface for the embedded processor.

The connector part number is Molex Micro Fit 43020-1000 with male pins. The mating connector is a Molex Micro Fit 043025-1000 and female pins.

GPIO Connector

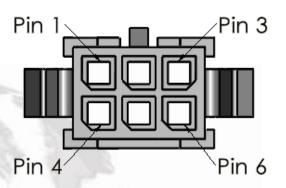


TABLE B: GPIO PIN OUT		
PIN	SIGNAL	
1	GPIO4	
2	GPIO3	
3	GSC INT	
4	GPIO2	
5	GPIO1	
6	GND	

The GPIO connector provides four 3.3V logic level input/output pins directly connected to the Gateworks GW7100.

They are used for different functions depending on the configured mode.

The connector also provides the internal GW7100 Gateworks System Controller Interrupt pin.

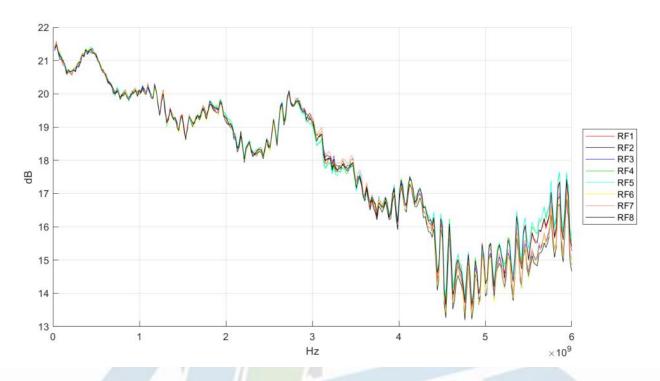
The connector is a Molex Micro Fit 43020-0600 with male pins. The mating connector is Molex Micro Fit 43025-0600 with female pins.

PRELIMINARY

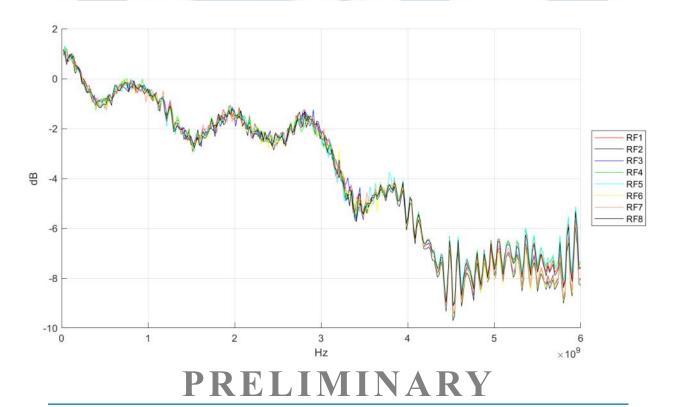




S21 Array Inputs to Output Port 1 (Output LNA Enabled)

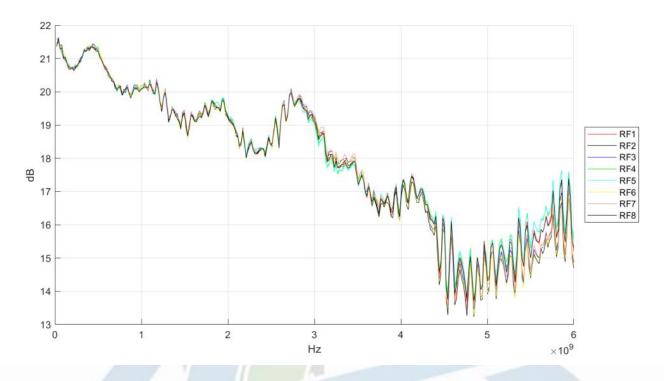


S21 Array Inputs to Output Port 1 (Output LNA Bypassed)

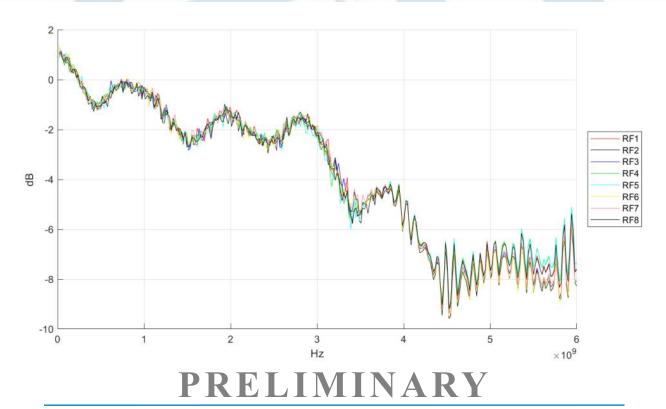




S21 Array Inputs to Output Port 2 (Output LNA Enabled)

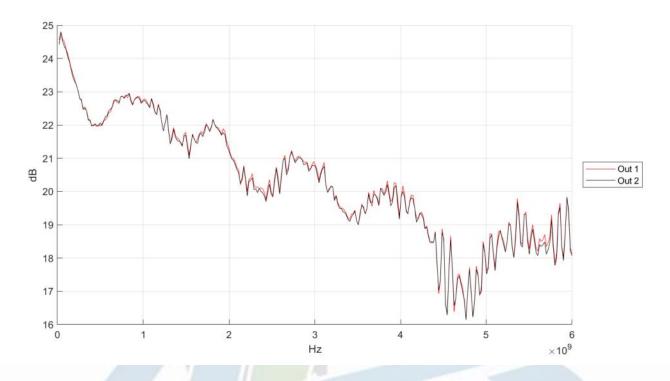


S21 Array Inputs to Output Port 2 (Output LNA Bypassed)





S21 Reference Input to Output Ports (Output LNA Enabled)



S21 Reference Inputs to Output Ports (Output LNA Bypassed)

